REMARKS

Claims 1, 3, 4, 8, 12-15 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent no. 6,330,657 B1 to Col, et al., ("Col") in view of Shang et al., U.S. Patent No. 5,764,971 ("Shang"); Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Col in view of Shang and further in view of Hennessy and Patterson, Computer Architecture – A Quantitative Approach, 2nd Edition, 1996 ("Hennessy"); Claims 6, 7, 10, 11, 17, 20 and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Col in view of Shang and further in view of Intel Architecture Optimization Reference Manual ("Intel"); Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Col in view of Shang and further in view of Phillips et al., U.S. Patent No. 6,038,652 ("Phillips"); and Claim 18 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Col in view of Shang and further in view of Makineni et al., U.S. Patent No. 6,321,327 B1 ("Makineni").

Claims 1-5, 7-16 and 18- 22 remain in this application. By this amendment, claims 1, 7, 10, 11 and 12, 18 and 20 are amended. Claims 6 and 17 are canceled. Reconsideration and allowance of the claims in view of the above-amendments and the remarks that follow is respectfully requested.

Claims 7, 10, 11, 12, 18 and 20 have been amended to conform with the Examiner's comments regarding the abbreviation of "floating-point".

Independent claims 1 and 12 have been amended to clarify that the claimed invention forces the issuing of at least two of microinstructions in parallel. Applicants note that pending claim 10 had a similar forcing limitation. Applicants respectfully submit that this amendment overcomes the Examiner's rejection under 35 U.S.C. § 103(a) over Col in view of Shang associated with claims 1, 3, 4, 8, 12-15 and 19 and places the pending claims in allowable form. Support for this amendment can be found in Figure 4 and the corresponding description in the specification. The remaining pending claims depend from these independent claims and are now, thus, in allowable form.

The Examiner stated that it would have been obvious to modify Col's system such that it employs exception detection among microinstructions as taught by Shang. The Applicants respectfully submit that an important innovative feature of the present invention that is not taught by Col or Shang is the *forcing* of the operations to execute in lockstep. As noted in the specification, Applicants disclosed and incorporated by reference in a previously co-pending application entitled, "Method And Apparatus For Implementing Two Architectures In A Chip" (and now allowed patent U.S. No. 09/496,845), a mechanism for

the forcing of the microinstructions to issue in parallel. Col merely allows for the parallel execution of instructions – Col does not require the forcing of the instructions. (*See e.g.,* Col col. 15, lns. 35-65). Neither Col nor Shang teach or suggest this feature of the claimed invention.

In addition, by forcing lockstep movement of the micro-operations, the claimed invention does away with the requirement for the extra storage that was required by the prior art. As noted by the Examiner, Col does not teach exception handling; thus, Col does not disclose how to cure an exception that occurs during parallel issue. Indeed, Col does not contemplate or disclose the temporary storage that is required by Shang. Shang discloses out of order execution (*See e.g.,* col. 5, lns. 5-35), where the execution of microinstructions requires the earlier executed instructions to be placed in a temporary storage. If later executed instruction have exception, then the instructions are not moved to permanent storage. In the present invention both instructions are executed together – if either instruction has exception, the exception handler takes control; thus removing the need for temporary storage. The combination of Col and Shang would still require the results of the microinstructions to be written to temporary storage. The desire to implement systems and methods to emulate instructions without the use of temporary storage was described in the Background section of the present application as one of the major shortcomings of the prior art. (*See e.g.,* Background of specification). The combination of Col and Shang requires temporary storage, and thus does not teach how to overcome the problems solved by the claimed invention.

Therefore, the combination of these references does not provide a system or method for emulating instructions and the handling of exceptions with existing hardware, as claimed in the presently amended claims. For example, the references relied upon by the Examiner, singularly or in combination, do not disclose, suggest or make obvious the forcing of the micro-operations, nor do the references teach or disclose the emulation of instructions without the use of temporary storage, a noted problem associated the prior that is present in both references. Applicant's respectfully submit that the combination of the two references does not make the innovations of the claimed invention obvious, and request the Examiner withdraw this rejection and allow the claims.

CONCLUSION

In view of the above amendments and remarks, Applicants respectfully assert that the application is in condition for allowance. Prompt reexamination and allowance of claims 1-5, 7-16 and 18-22 is respectfully requested. Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

Date: **July 1, 2003**

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